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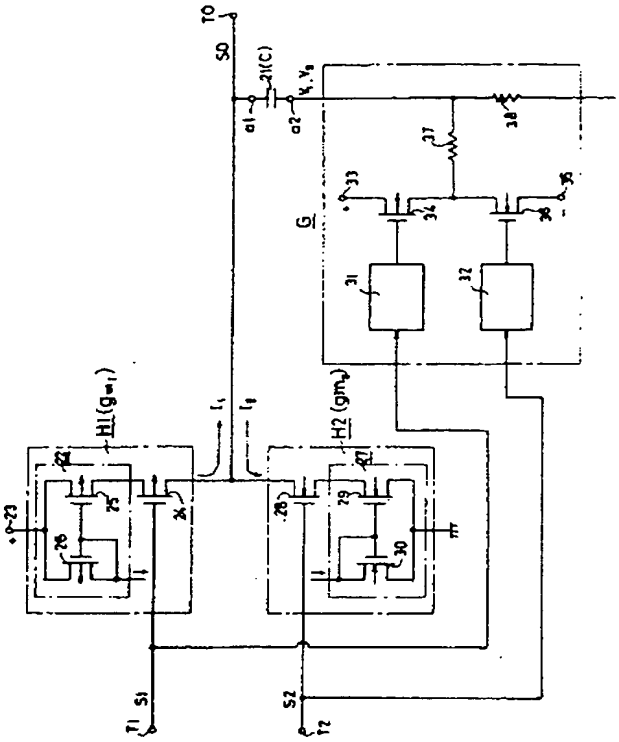
TITLE : PRIMARY LOW-PASS FILTER



ABSTRACT : PURPOSE: To obtain a circuit suitable for IC, by constituting the primary low-pass filter with the circuit which supplies a current to the capacity element by the input signal, the circuit which absorbs the current from the capacity element, and the circuit which supplies a voltage to the capacity element.

CONSTITUTION: Current supply circuit H1 and current absorbing circuit H2 are connected to terminal a_1 of capacity circuit 21. Circuit H1 is controlled by input signal S_1 to supply current I_1 to element 21. Circuit H2 absorbs current I_2 from element 21 by the control of the second signal S_2 having the polarity opposite to signal S_1. Voltage generating circuit G is connected to the other terminal a_2 of element 21. Circuit G generates voltage V_1 by signal S_1 and generates voltage V_2 of the opposite polarity by signal S_2 and supplies them to element 21 through terminal a_2 and outputs output signal SO from terminal TO. Signals S_1 and S_2 are given at different times; and if absolute values of currents I_1 and I_2 and voltages V_1 and V_2 are made equal to each other respectively, the capacity of element 21 is small, and it is constituted with an integrated circuit.

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A Design of a Compact 2GHz -PLL with a New Adaptive Active Loop Filter Circuit

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Abstract

This paper describes a design of a compact active loop filter for Phase-Locked-Loop (PLL) with adaptive biasing technique. Using the new loop filter, the PLL can automatically adjust the loop bandwidth and damping factor to the frequency of the reference clock. Moreover, the new LPF can decrease the capacitance value to 1/10-1/20 of conventional one. A test chip was fabricated in 0.15μm-CMOS process. The total chip area of the PLL is reduced to 1/2 of previous one. The jitter performance is almost equal to conventionally biased PLL.

I. Introduction

PLL is very popular circuit component of system LSI. It is not too much said that every system LSI has at least one PLL circuit. Recently, the most general PLL is charge-pump type PLL (CP-PLL) which has digital phase frequency detector. The CP-PLL has limitation of loop bandwidth due to its digital component [1]. The highest loop bandwidth is about 1/10 of the frequency of the reference clock. If the reference frequency is low, the CP-PLL must have a large filter which cannot be integrated in LSI chip. Even if the PLL is integrated in the chip, it costs much to take large chip area [2]. Particularly it is critical in deep quarter micron process. On the contrary, off-chip loop filter is affected by noise. Moreover, the circuit of such outside loop filter becomes more complex, if the PLL has various loop bandwidths. Thus, new technologies are needed to reduce filter area and circuit complexity.

II. Loop Filter Circuit

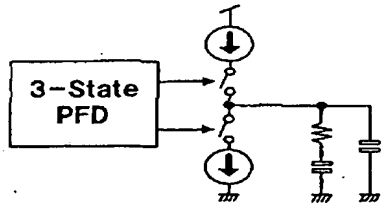


Fig.1 The Conventional Loop Filter

A conventional charge pump and a loop filter circuit of PLL are shown in Fig. 1. Generally, the filter is passive because the charge pump circuit (CP) has already had a role of an opamp. One of the drawbacks of the CP is the mismatch between charge and discharge current. The error is suppressed by cascode current sources. However recent decrease of the supply voltage makes it difficult to use cascode current sources.

A charge pump circuit with an active loop filter is shown in Fig.2.

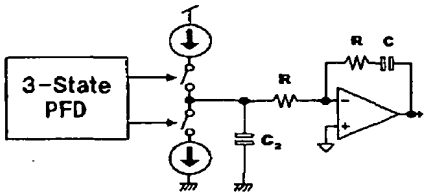


Fig.2 The Active Loop Filter

By using an opamp, the output voltage of the CP is constant. Stabilizing the output voltage can make the current error of the CP minimum. Hence we can easily minimize the output jitter over wide VCO oscillation range. Although the active filter shown in Fig.2 is suitable for low voltage operation, this type of filter dissipates much power in order to supply current flow from the CP by using a high slew rate opamp.

Another disadvantage of using the active filter is increase of the number of resistors. The filter needs twice number of resistors and switches compared to the passive filter to cover various bandwidth of the PLL. Thus, we need a new low power active filter which is able to change filter characteristics easily.

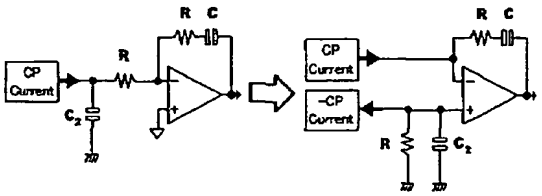


Fig.3 The first conversion of the Active Filter

Fig.3 shows the first conversion of the active filter [3]. If the resistors in each circuit have the same value, two filters are equivalent. But the converted filter needs two charge pump circuits.

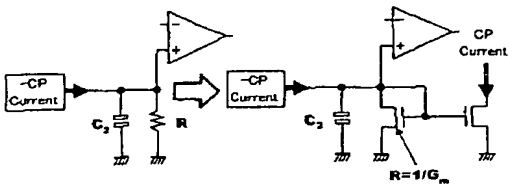


Fig.4 The generation of the opposite current flow

In order to eliminate one of the CP circuits, we change the resistor connected to the positive input of the opamp to a MOS resistor. The current flow into the MOS resistor is mirrored by a current mirror circuit so that the circuit makes opposite current flow (shown in Fig.4).

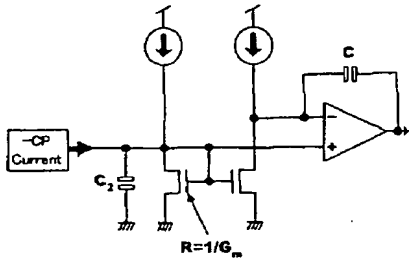


Fig.5 New Active Loop Filter

Finally, we get a new active loop filter shown in Fig.5.

Assuming the resistance of the MOS resistor is equal to the resistance of the original active loop filter, the transfer function (F(s)) of the new filter is shown as follows.

$$F(s)=\frac{1+sCR}{sC(1+sC_2R)}$$

The transfer function of the new active loop filter is exactly the same as the original one.

The new active filter uses the current mirror circuit. Hence, we can reduce the filter capacitance by changing the mirror ratio. If we set the mirror ratio to A:1 as shown in the Fig.6, the capacitance of the filter can be reduced to 1/A.

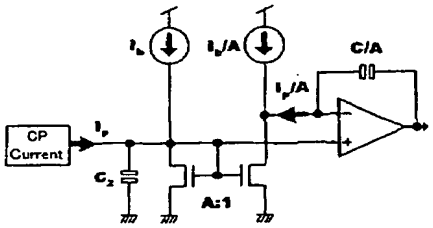


Fig.6 Reduction of the Capacitance

The current flowing into the opamp is also reduced to 1/A. It means that we don't need a high slew rate opamp.

The suitable value of A is determined by the condition that C/A is equal to C_2, because C_2 is independent of A.

We can reduce the capacitance of C_2 by making the resistance of the MOS diode large. However, increase of the resistance means decrease of both I_p and I_b. The excessive decrease of I_p can cause large jitter of the PLL. Proper upper limit of A is 20.

III. Active Filter Design

The performances required to the opamp in the Active loop filter are as follows.

1. Enough slew late to supply charge pump current.
2. Enough GB product not to degrade PLL response.
3. High PSRR not to degrade jitter performance.

The new active loop filter can solve the first subject. By using the new active filter, the slew rate of the opamp is reduced to 1/10 of conventional one. Considering the 2nd and the 3rd subjects, we chose a folded cascode type opamp.

The PLL response taking into account of the non-ideal effects of the opamp is somewhat complex. Thus, we approximate the filter response by the following simple transfer function.

$$F(s)=F_i(s)/(1+1/H_{amp}(s))$$

Here F(s) is the filter response including non-ideal effects of the opamp, $F_i(s)$ is the ideal filter response, and $H_{amp}(s)$ is the transfer function of the opamp.

In this case, we found that the opamp transfer function does not affect the filter response, if the GB product of the opamp is over ten times higher than the PLL loop

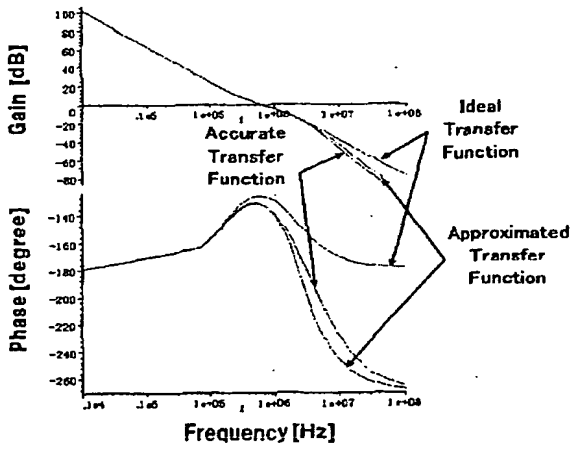


Fig.7 The Comparison of the Filter Frequency Characteristics

bandwidth. Fig.7 shows the comparison of the frequency characteristics of the accurately calculated transfer function, the approximated transfer function and the ideal transfer function.

The approximated function has the most severe phase margin in the three responses. We can use the approximated equation for easy filter design.

IV. Adaptive Biasing

The other characteristic of the new active filter is using the MOS resistor to set a damping factor. Changing the bias current of the MOS resistor, we can easily adjust the damping factor to any loop bandwidth. Adaptive biasing is very useful way to make the compact PLL, because it doesn't need a reference circuit such as Band Gap Reference. The circuit reported previously realizes only 2^{nd}-order adaptive PLL[4]. The new active filter can realize 3^{rd}-order adaptive PLL.

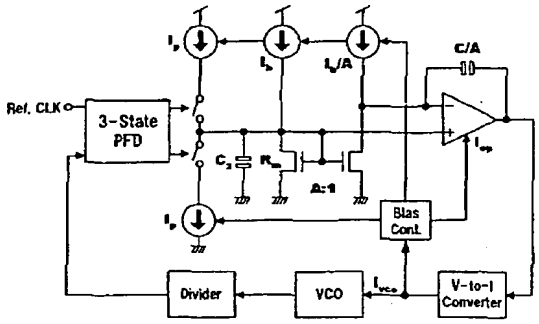


Fig.8 The Block Diagram of Adaptively Biased PLL

The block diagram of the new adaptive PLL is shown in Fig 8. The charge pump current(I_p), MOS resistor bias current(I_b) and opamp bias current(I_{op}) are generated to be proportional to the VCO bias current(I_{vco}). The damping factor and loop bandwidth are approximately calculated by the following equations.

$$\omega_n = \left(\frac{I_p K_o}{2\pi C}\right)^{1/2} \qquad \zeta = \frac{CR_m}{2}\left(\frac{I_p K_o}{2\pi C}\right)^{1/2}$$

Here K_o is the product of the VCO gain and the conversion gain of V-to-I converter(K_v). As well known , the resistance of the MOS diode(R_m) is proportional to $I_b^{-1/2}$. The damping factor(ζ) is proportional to the product of $I_p^{1/2}$ and R_m. Therefore, ζ is constant as in the following equations.

$$\zeta \propto I_p^{1/2} \times R_m \propto I_p^{1/2} \times I_b^{-1/2} \propto I_{vco}^{1/2} \times I_{vco}^{-1/2} = \text{constant}$$

The loop bandwidth(ω_n) is proportional to $Ip^{1/2}$. If the reference frequency(ω_{ref}) is low, it becomes difficult to satisfy the bandwidth limitation $\omega_{ref}/10 > \omega_n$. In the actual adaptive bias circuit, the lower the reference frequency is, the smaller the bias current of every circuit in the PLL. In such a case, the bias conditions of transistors go into the weak inversion region.

The transconductance of the V-to-I converter shown in Fig.9 has constant transconductance in strong inversion region. It has linear characteristics against input voltage in weak inversion region. Fortunately, this nonlinear effect alleviates the bandwidth limitation. Because the frequency of the VCO circuit is determined by I_{vco}/C_{para}, where C_{para} is parasitic capacitance and I_{vco} is the current flow into the inverter chain of the VCO respectively. Here C_{para} is the constant parameter. Then, VCO gain is constant especially in low oscillation frequency.

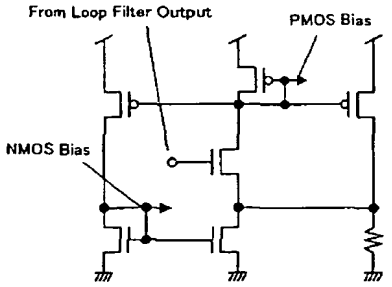


Fig.9 The Circuit Schematic of the V-to-I converter

The factor to change PLL loop bandwidth(ω_n) is I_p and the conversion gain of the V-to-I converter(K_v). We can get the following relationship in weak inversion operation:

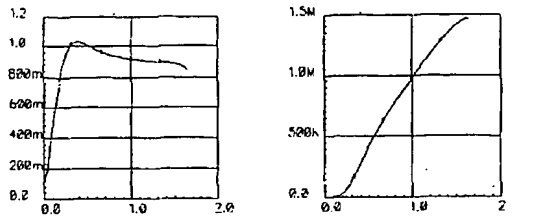
$$\omega_n \propto (I_p \times K_v)^{1/2} \propto (I_{vco} \times I_{vco})^{1/2} = I_{vco} \propto F_{VCO} \propto F_{ref}$$

Here, F_{VCO} is the oscillation frequency of the VCO and F_{ref} is the reference frequency. Thus the loop bandwidth of the PLL is proportional to the reference frequency in low VCO oscillation range.

V. Simulation

We have modified the original PLL reported in ISSCC2002[5] to get an adaptively biased PLL in 0.15μm CMOS process.

We simulated the test circuit to measure the relationship between the V-to-I input voltage and the PLL response. The characteristics of ω_n and ζ are shown in Fig.10(a) and Fig.10(b) respectively. Fig.10 shows almost constant damping factor and the linear response of the loop bandwidth within normal operation range of the V-to-I converter.



(a) V-to-I Input Voltage vs ζ (b) V-to-I Input Voltage vs ω_n

Fig.10 Simulated PLL Response vs. V-to-I Input Voltage

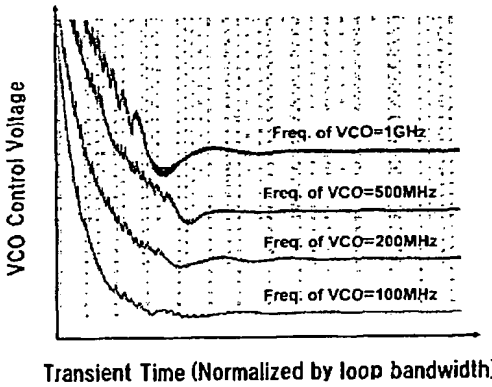


Fig.11 The simulation results of transient responses of the PLL

Fig.11 shows the simulation results of transient responses of the PLL from 100MHz to 1GHz of VCO output frequency. The divider ratio is fixed to 24. Note that the each waveform was shifted adequately for clear understanding of its response. Keeping almost constant response, the new PLL can operate without any change of the circuit within ten times reference frequency variation.

VI. Chip Layout and Measurement Results

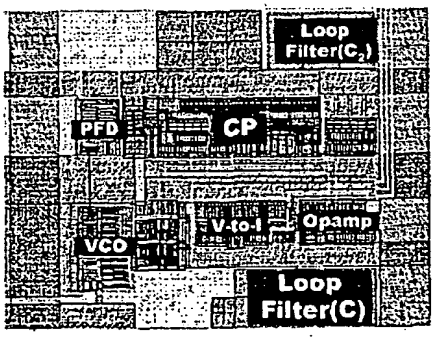


Fig.12 The Layout Pattern of Test Circuit

The layout pattern of this circuit is shown in Fig 12. The chip area is reduced to 1/2 of the previous one. The measured chip performances are shown in Table. I. Jitter performance is almost equal to the conventionally biased PLL.

Table. I The Measured Performances of Adaptive Bias PLL

Supply Voltage		1.2V	
Output Freq.		2GHz-250MHz	
Power Consumption		7.6mW@2GHz-output	
Chip Area		This PLL	Prev. PLL
		0.0676mm²	0.135mm²
Output Jitter (3 σ)	Out Freq.	Adaptive Bias	Conv. Bias
	1.92G	0.95%	0.91%
	1.68G	1.18%	1.12%
	1.44G	1.33%	1.24%
	1.20G	1.54%	1.33%

VII. Conclusions

The new compact active loop filter for PLL is successfully developed. The new technique can reduce the filter size to 1/10-1/20. Collaborating with the adaptive biasing technique, total circuit size of the PLL is typically reduced to 1/2 of conventional one while keeping good jitter performance.

Acknowledgement

The authors thank to Dr. Takashi Morie for valuable discussions on this paper.

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